The Effect of Coating and Potting on the Reliability of QFN Devices

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Abstract

The fastest growing package types in the electronics industry today are Bottom Termination Components (BTCs). While the advantages of BTCs are well documented, they pose significant reliability challenges to users.

One of the most common drivers for reliability failures is the inappropriate adoption of new technologies. This is especially true for new component packaging like BTCs. Obtaining relevant information can be difficult since information is often segmented and the focus is on design opportunities not on reliability risks. Most users have little influence over component packaging and most devices offer only one or two packaging styles. And, when faced with challenges, users typically fall back on tried and true solutions that may not work for new packaging. This has already occurred with BTC components. Commonly used conformal coating and potting processes have resulted in shortened fatigue life under thermal cycling conditions.

Why do conformal coating and potting reduce fatigue life? This paper details work undertaken to understand the mechanisms underlying this reduction. Verification and determination of mechanical properties of some common materials are performed and highlighted. Recommendations for material selection and housing design are also given. Basically, the lack of a compliant lead structure makes BTC devices more susceptible to PCB warpage related failures so proper precautions must be taken to ensure adequate fatigue life for high reliability applications.

Introduction

Since the advent of Surface Mount Technology (SMT) in the mid 1970's the electronics industry has continued to evolve from a packaging perspective by continually reducing the size of the component packages. First there were leadless chip carriers, later Ball Grid Arrays, Chip Scale Packages, and more recently Bottom Terminated Components. These package types are primarily designed for low cost applications or for products where a short lifetime is acceptable (e.g. cell phones). However, designers have been incorporating BTCs into products that expected to survive environmental stresses for prolonged periods of time. This paper will address the effects that conformal coating and potting have on these BTC packages and offer a new technology that may provide additional reliability benefit.

What is a QFN?

A QFN (Quad **F**lat Pack **N**o Lead) or **Q**uad **F**lat **N**on-Leaded has been called the poor man's ball grid array (BGA). It has also been identified as a Leadframe Chip Scale Package (LF-CSP), MicroLeadFrame (MLF),

MLP = molded lead package, LPCC – Leadless Plastic Chip Carrier, QLP = Quad Leadless Package, HVQFN = heatsink very thin QFN.

This package type utilizes an overmolded leadframe with bond pads exposed on the bottom and arranged along the periphery of the package as shown in Figure 1.

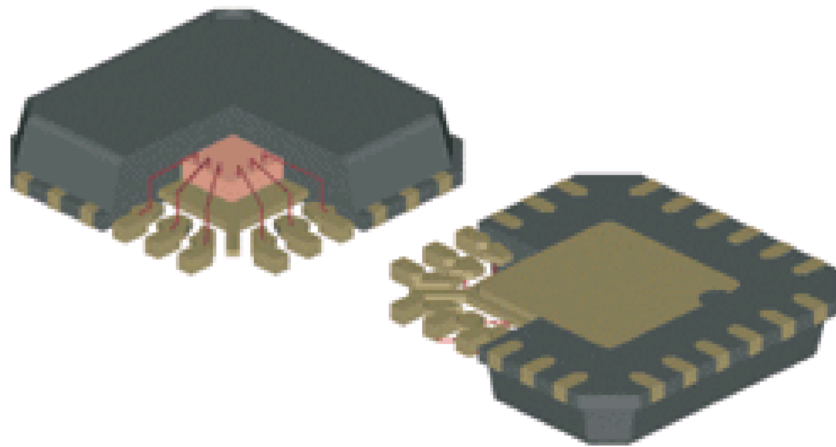


Figure 1 – Typical QFN Cross Section

The package was developed in the early to mid-1990's by Motorola, Toshiba, Amkor, etc. and was standardized by JEDEC/EIAJ in the late-1990's. It is the fastest growing package type in the electronics industry today.

Advantages

There are several distinct advantages for the selection of BTC/QFN packaging for current applications. The elimination of leads provides lower resistance, lower inductance, higher performance and higher package densities. The packaging configuration has a more direct thermal path with larger area:

Die→ Die Attach → Thermal Pad → Solder → Board Bond Pad

Also, the θJa for the QFN is about half that of a leaded counterpart (as per JESD-51) which in turn allows for a 2X increase in power dissipation capability. The rate of heat transfer between two bodies may be quantified in terms of the thermal resistance between them. In the simple model mentioned above, the over-all thermal resistance between the die and the surroundings of the device, θja ('ja' stands for 'junction-to-ambient') is the sum of two thermal resistances: 1) the thermal resistance between the die and the package, θjc ('jc' stands for 'junction-to-case'); and 2) the thermal resistance between the package and the surroundings, θca ('ca' stands for 'case-to-ambient'). Table 1 summarizes this comparison with other packaging formats.

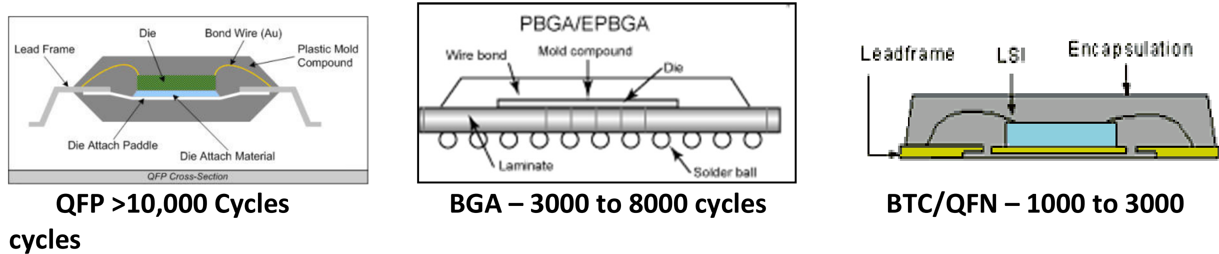
Package Type	Body Size (mm)	Leads	Height (mm)	Max Die Size	PCB Area	θ Ja
QFN	7 x 7	48	1.00 max	203 x 203 mils	49 mm²	27
TQFP	7 x 7	48	1.20 max	190 x 190 mils	81 mm²	55
QFN	5 x 7	38	1.00 max	124 x 202 mils	35 mm²	34
TSSOP	4.4 x 9.7	38	1.10 max	108 x 207 mils	62 mm²	73
QFN	5 x 5	16	1.00 max	124 x 124 mils	25 mm²	37
QSOP	3.9 x 4.9	16	1.75 max	86 x 120 mils	31 mm²	112

Table 1 – Theta Ja Comparison of QFN package to Other packaging Formats

At higher operating frequencies, inductance of the gold wire and long lead-frame traces will affect performance of the circuit. Another advantage of the QFN package is that its inductance is half its leaded counterpart because it eliminates gullwing leads and shortens wire lengths.

Disadvantages

Conversely, the QFN package also inherently has increased power density, manufacturability issues and is more susceptible to thermal mechanical fatigue. The transition from older packaging approaches (e.g. Quad Flat Packs (QFP) to Ball Grid Array (BGA) to BTC/QFN has seen a declining level of ability to survive temperature cycling as illustrated in Figure 2. The cycles to failure identified are as a result of -40 to +125 C thermal cycles.



QFP >10,000 Cycles **BGA – 3000 to 8000 cycles** **BTC/QFN – 1000 to 3000 cycles**

Figure 2 – Comparison of Thermal Cycles to Failure for QFP, BGA, and BTC/QFN packages

On numerous equations, DfR has documented that the increased die to package ratio in QFN and CSP packages has resulted in a reduction in fatigue life. Figure 3 illustrates this concept. As the ratio increases, the fatigue life decreases, e.g. from a 40% ratio where the fatigue life is 8000 hours to a ratio of 70% where it is approximately 1000 hours.

As DfR has shown, the Bottom Terminated Component (BTC-QFN) has significant positives and negatives with respect to using this type of package in high reliability applications.

Another area that is of concern is the use of conformal coatings or potting compounds and their impacts on BTC packages.

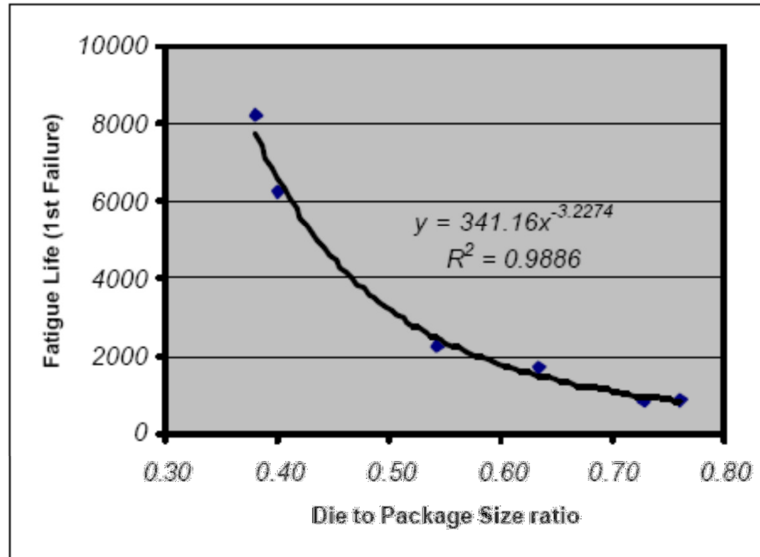


Figure 3 – Ratio of Die to Package Size versus Fatigue Life.

Impact of Conformal Coating or Potting

The use of underfills, potting compounds and thick conformal coatings can greatly influence the failure behavior under thermal cycling. Anytime a material goes through its glass transition temperature problems tend to occur. Conformal coating should also not bridge between the PCB and the component. Underfills designed for enhancing shock robustness do not tend to enhance thermal cycling robustness. As such, it is critical to select the appropriate underfill as a function of the application.

Potting materials can also cause PCB warpage and tensile stresses on electronic packages that greatly reduce time to failure.

Thermal cycling

Care must be taken when using conformal coating over QFN or BTC as the coating can infiltrate under the QFN. The small standoff height allows the coating to cause lift of the package if it does permeate under the package. Hamilton Sundstrand found a significant reduction in time to failure during thermal cycling (-55 / 125C) for uncoated versus coated QFN packages. The uncoated devices failed between 2000 and 2500 cycles while the coated packages failed between 300 and 700 cycles.

These failures are also driven by solder joint sensitivity to tensile stresses where the damage evolution is far higher than for shear stresses.

Why did conformal coating affect thermal cycling performance? DfR explored verification and determination of mechanical properties of the coating specifically addressing; Elastic Modulus as a function of temperature; Glass Transition Temperature; and Coefficient of Thermal Expansion of the materials. Table 2 shows typical characteristics of acrylic conformal coating. Note that the Tg of the material is 15C and the modulus is 1260 psi (8.7 MPa).

	Property	Value
Physical	Continuous Use Temp. Range °C	-65 +125
	Thermal Shock Test[7]	Passes
	Flammability[8] (self extinguishing)	Yes
	TCE in/in/°C[9]	5.5×10^{-5}
	Young's Modulus[10] psi	1260
	Tg °C[11]	15
Electrical	Dielectric Constant[12]	2.5
	Dissipation Factor[13]	.01
	Dielectric Withstand[14] (volts)	>1,500
	Insulation Resistance[15] (teraohms)	800
	Moisture Resistance[16] (gigaohms)	60

Table 2 – Acrylic Conformal Coating Material Properties

Figure 4 shows the change in Elastic Modulus as a function of coating thickness and temperature. The samples were coated with a typical acrylic conformal coating material and were measured using Dynamic Material Analysis (DMA). DMA is method of applying an oscillating force to a sample and analyzing the material's response to that force (Dynamic Mechanical Analysis: A Practical Introduction, K. P. Menard, CRC Press, 1999). Through use of an oscillating force, the material can be subjected to a range of frequencies (0.1 Hz to 300 Hz). It is well known that the response of polymers will change dependent upon the frequency applied

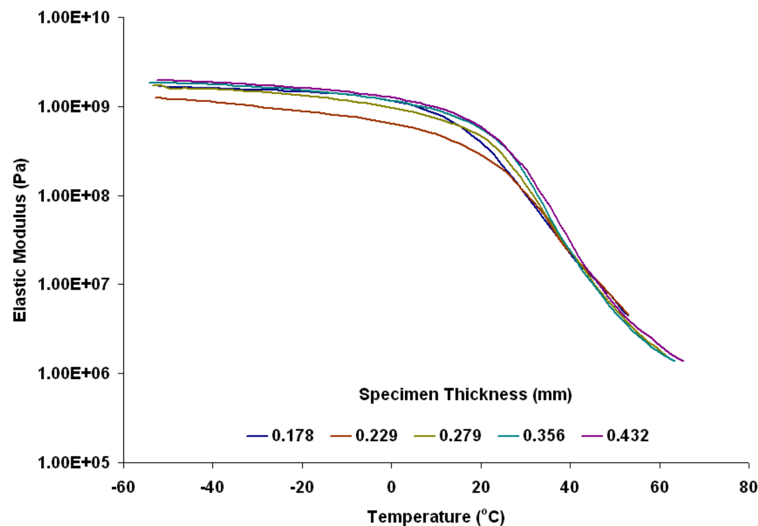


Figure 4 – Elastic Modulus Compared to Conformal Coating Thickness and Temperature.

Similarly, Figure 5 shows the impact of increasing temperature on the Tg of the material and the resultant stress that would be applied to the BTC/QFN package. The measurement was obtained using

Thermomechanical Analysis (TMA), a technique used in thermal analysis, a branch of materials science which studies the properties of materials as they change with temperature.

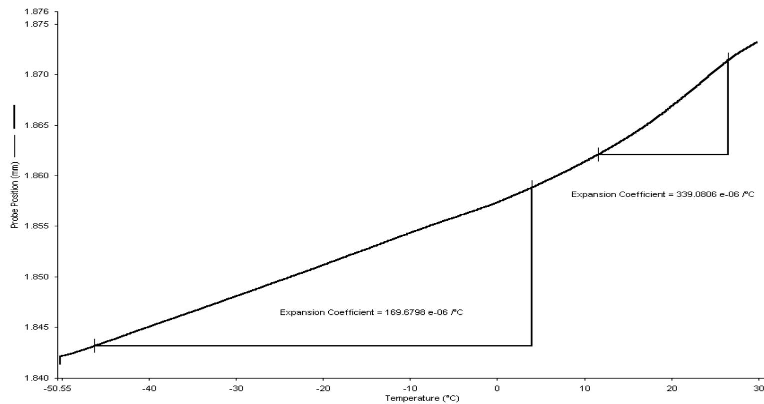


Figure 5 – Impact of Tg on Acrylic Coating

Potting

Ideally the Coefficient of Thermal Expansion (CTE) of the potting material should be as close to that of the CCA as possible, usually in the 20 to 30 ppm/°C range. The larger the CTE, the more compliant the potting must be to limit the stresses imparted to the CCA. Also, potting should generate hydrostatic pressure (equal on all sides) of the circuit card as this prevents warping of the CCA as the potting expands. Excessive warping will greatly reduce time to failure and may cause overstress failures resulting in modifications to the housing. The glass transition temperature (Tg) is the temperature at which the potting compound changes structure and becomes harder. Some polyurethane materials have Tg's below –50 C. This means less stress as the potting compound does not become hard at those temperatures, so it can deform rather than putting pressure on the components.

Figure 6 illustrates this change of Modulus and CTE with respect to temperature for a material with a CTE of 120 ppm.

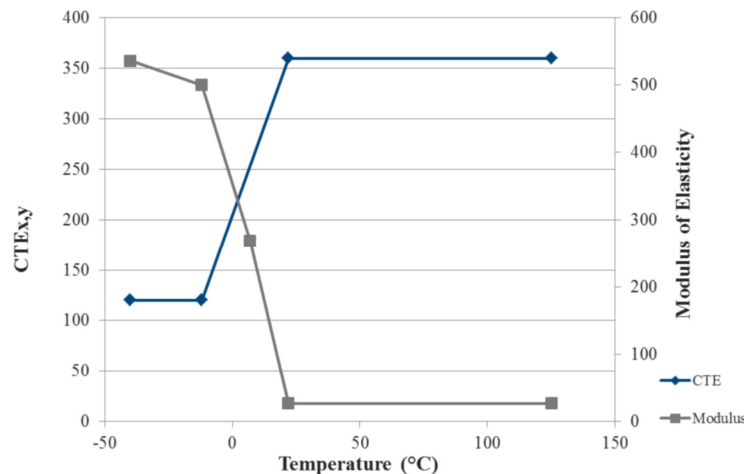


Figure 6 – CTE and Modulus Change as a Function of Temperature

DfR observed that BTC/QFN failures occurring very rapidly during temperature cycling (-40 to 105C) with urethane based potting material with all units failing at the 100 cycle inspection point. The packages had good quality joints with sufficient solder thickness. (2.5 to 3 mils standoff).

PWB Warpage

Potting shrinkage was the issue DfR deemed the most damaging to BTC packages. Figure 7 shows a model of the deflections observed in a PCB when the unit is potted and subjected to a thermal cycle.

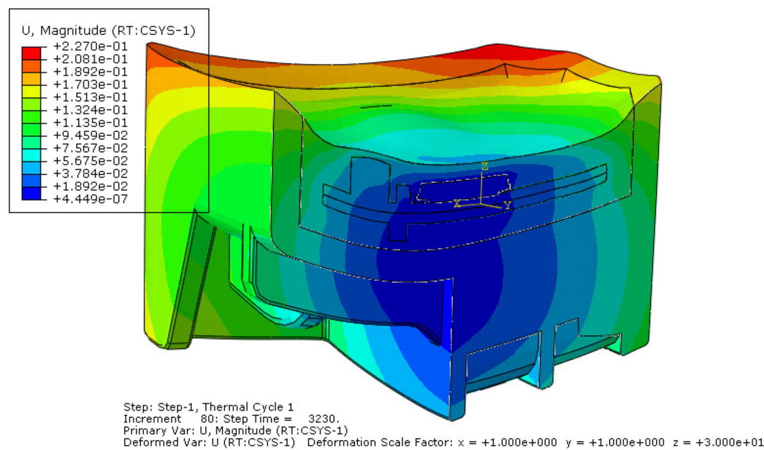


Figure 7 – Deformation of a PCB in a Housing that is Potted

QFN Warpage

Similarly, the QFN package will also see deformations as a result of the potting compound. Figure 8 shows an unpotted QFN on the left and a potted QFN on the right. Clearly, the warpage is an order of magnitude higher for the potted package with the deformation concentrated over corner solder joints.

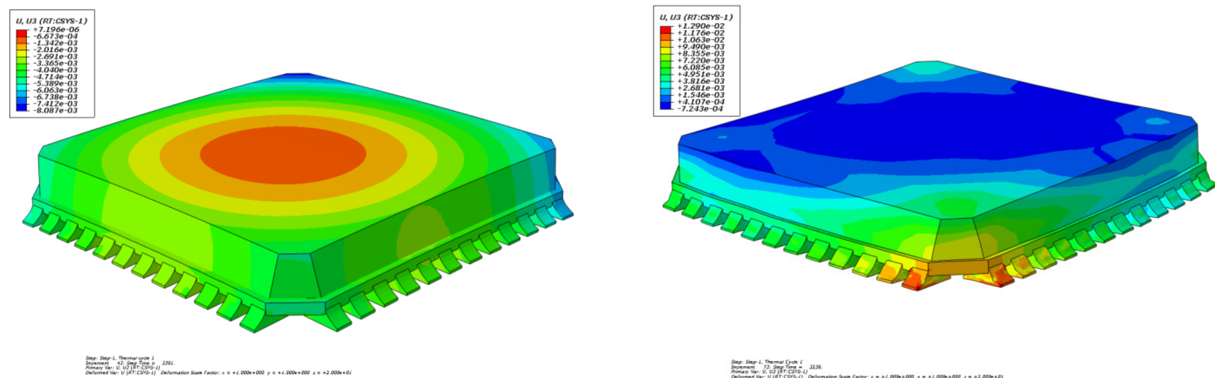


Figure 8 – Comparison of Stresses on Unpotted QFN (Left) and Potted QFN (right)

Solder Stresses

Very high stresses were noted during the cold temperature dwell. In Figure 9 the image on the left shows the temperature transition from hot (lower stress) to cold (higher stress). The image on the right shows where the stresses impact the solder joints on the QFN package, particularly those in the corners.

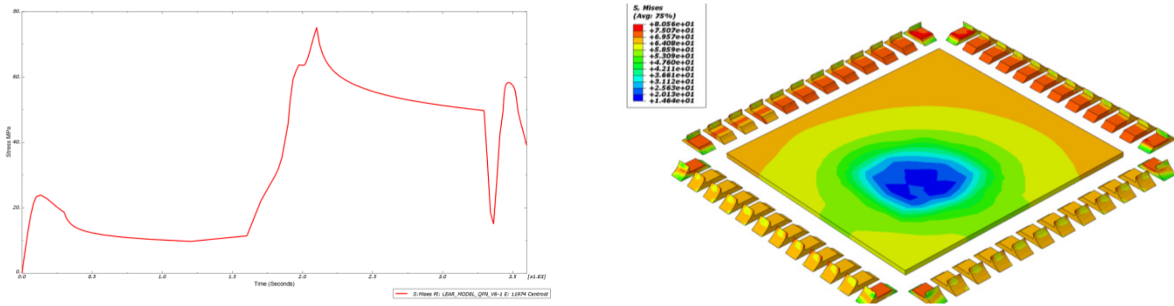


Figure 9 – Hot to Cold Stress Transition and Impact on Solder Joints

Creep Strains

In materials science, creep is the tendency of a solid material to slowly move or deform permanently under the influence of stresses. It occurs as a result of long term exposure to high levels of stress that are below the yield strength of the material. Creep is more severe in materials that are subjected to heat for long periods, and near melting point. Creep always increases with temperature. Figure 10 (left) is the stress observed on an unpotted device while the right image is for a potted component. Clearly, the stress levels observed for the potted configuration are significantly higher. The higher the creep strains the shorter time to failure. More energy is required to cause cold temperature creep and therefore it is more damaging.

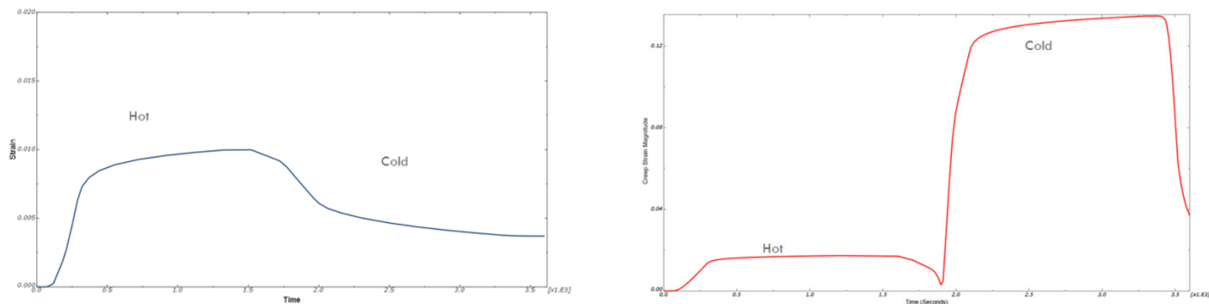


Figure 10 – Creep Stress (unspotted left and potted right) Comparison

Conclusions

The lack of a compliant lead structure makes BTC/QFN devices more susceptible to PCB warpage related failures. The mechanical properties of the potting material have a profound impact on the reliability of the package. The user needs to pay strict attention to the glass transition temperature (Tg) of the package and PCB. The modulus should be specified above and below the Tg and the CTE should be specified above and below the Tg.

The mechanical design of the housing may provide a surface to which the potting material can pull against when shrinking causing PCB warpage and should be designed to provide as close to a hydrostatic pressure as possible (equal pressure on all sides).